the structures shown in FIGS. **8** to **10**, a gate capacity can be reduced to thus make a higher speed operation possible. And, those skilled in the art will recognize that many variations of such embodiments exist. Such variations are intended to be within the scope of the present invention and the appended claims.

What is claimed is:

1. A power MOSFET having;

a plurality of base regions;

source regions formed in the base regions;

a first drain region of a first semiconductor disposed between the base regions to form a pn-junction between the base and first drain regions, the first drain region having a convex portion; and

a second drain region of a second semiconductor having a bandgap wider than the first semiconductor disposed on and directly contacted with the convex portion to form a hetero-junction between the first and second semiconductor.

2. The power MOSFET of claim **1**, further comprising a drain contact region of the second semiconductor having an impurity concentration higher than that of the second drain region, formed on the second drain region to have a position of the drain contact region higher than that of the source region.

3. The power MOSFET of claim **2**, wherein the base regions are formed on a surface of a semiconductor region of opposite conductivity type to that of the base regions, and a buried region of the opposite conductivity type to that of the base regions is formed at a bottom of the semiconductor region which acts as a third drain region.

4. The power MOSFET of claim **2**, wherein said semiconductor region is a diffused region disposed in an epitaxial layer, the epitaxial layer having the same conductivity type as that of the base regions to form a pn-junction between said semiconductor region and said epitaxial layer.

5. The power MOSFET of claim **2**, wherein the base regions are formed on a surface of a semiconductor substrate of an opposite conductivity type to that of the base regions.

6. The power MOSFET of claim **1**, wherein the base regions are formed on a surface of an epitaxial layer formed on a top surface of a high impurity concentration substrate of opposite conductivity type to that of the base regions, a first drain electrode is formed on a top portion of the second drain region, source electrodes are formed on the source regions, and a second drain electrode is formed on a bottom surface of the high impurity concentration substrate.

7. The power MOSFET of claim **6**, wherein a voltage applied between the second drain and source electrodes is lower than that applied between the first drain and source electrodes.

8. The power MOSFET of claim **1**, wherein the second semiconductor is formed of silicon carbide (SiC) and the first semiconductor is formed of silicon (Si).

9. A power MOSFET having a plurality of base regions, source regions formed in the base regions and a drain region formed between the base regions,

wherein the drain region has a convex portion and at least a part of the convex portion is formed of a wide bandgap semiconductor which has a wider bandgap rather than another portion of the drain region, the base regions are formed on a surface of an epitaxial layer which is formed on a top surface of a high impurity concentration substrate of opposite conductivity type to that of the base regions, a first drain electrode is formed on a top portion of the convex portion, source electrodes are formed on the source regions respectively, and a second drain electrode is formed on a bottom surface of the high impurity concentration substrate.

10. The power MOSFET of claim **9**, wherein a voltage applied between the second drain and source electrodes is lower than that applied between the first drain and source electrodes.

11. The power MOSFET of claim **9**, wherein the wide bandgap semiconductor comprises a high impurity concentration region serving as a wide bandgap contact region and a wide bandgap drain region having an impurity concentration which is lower than that of the wide bandgap contact region.

12. A power MOSFET having a plurality of base regions, source regions formed in the base regions and a drain region formed between the base regions,

wherein the drain region has a convex portion, sandwiched in between gate electrodes via insulating films, and at least a part of the convex portion is formed of a wide bandgap semiconductor which has a wider bandgap rather than another portion of the drain region.

13. The power MOSFET of claim **12**, wherein the base regions are formed on a surface of a semiconductor region of opposite conductivity type to that of the base regions, and a buried drain region of the opposite conductivity type to that of the base regions is formed at a bottom of the semiconductor region which acts as a part of the drain region.

14. The power MOSFET of claim **12**, wherein the base regions are formed on a surface of a semiconductor region of conductivity type opposite to that of the base regions, and a buried drain region of the opposite conductivity type to that of the base regions is formed at a bottom of the semiconductor region which acts as a part of the drain region.

15. The power MOSFET of claim **13**, wherein said semiconductor region is a diffused region disposed in an epitaxial layer, the epitaxial layer having the same conductivity type as that of the base regions to form a pn-iunction between said semiconductor region and said epitaxial layer.

16. The power MOSFET of claim **12**, wherein the base regions are formed on a surface of a semiconductor substrate of opposite conductivity type to that of the base regions.

17. The power MOSFET of claim **12**, wherein the base regions are formed on a surface of a semiconductor substrate of opposite conductivity type to that of the base regions.

18. The power MOSFET of claim **12**, wherein the base regions are formed on a surface of an epitaxial layer which is formed on a top surface of a high impurity concentration substrate of opposite conductivity type to that of the base regions, a first drain electrode is formed on a top portion of the convex portion, source electrodes are formed on the source regions respectively, and a second drain electrode is formed on a bottom surface of the high impurity concentration substrate.

19. The power MOSFET of claim **18**, wherein a voltage applied between the second drain and source electrodes is lower than that applied between the first drain and source electrodes.

20. The power MOSFET of claim **12**, wherein the wide bandgap semiconductor comprises a high impurity concentration region serving as a wide bandgap contact region and a wide bandgap drain region having an impurity concentration which is lower than that of the wide bandgap contact region.

21. The power MOSFET of claim **12**, wherein the wide bandgap semiconductor is formed of silicon carbide (SiC) and the other portion is formed of silicon (Si).

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